What is Claimed Is:

1. A multiport switch configured for controlling communication of data frames between stations, comprising:

a plurality of receive devices corresponding to ports on the multiport switch, each of the receive devices configured to receive data frames and transmit the data frames on an internal bus to an external memory interface;

a plurality of queues corresponding to ports on the multiport switch, the plurality of queues formed on a memory device that includes a write port and a read port to enable data to be written to and read from the memory device simultaneously, wherein each of the plurality of queues is configured to store frame header information received via the write port;

a scheduler configured to allocate time slots to the plurality of queues; and

a decision making engine configured to receive the frame header information in successive time slots via the read port and to generate data forwarding information.

2. The multiport switch of claim 1, comprising:

a read controller configured to transfer frame header information from the plurality of queues to the decision making engine via the read port,

wherein the scheduler is configured to allocate the time slots based on a predetermined priority and the read controller is configured to transmit frame header information to the decision making engine during the allocated time slots.

3. The multiport switch of claim 2, wherein the read controller is configured to transmit a request signal to the scheduler, the request signal indicating that a first queue has stored frame header information.

4. The multiport switch of claim 3, wherein:

each of the plurality of queues is assigned at least one time slot in a scheduling cycle and the scheduler is configured to allocate the time slot assigned to the first queue when a request signal associated with the first queue has been received, and

the read controller is configured to transmit the frame header information from the first queue to the decision making engine during the allocated time slot.

5. The multiport switch of claim 1, wherein the frame header information comprises a source address and destination address of the data frame.

6. The multiport switch of claim 5, wherein the frame header information includes virtual local area network (VLAN) information.

7. The multiport switch of claim 1, wherein the memory device comprises a plurality of synchronous random access memory (SRAM) devices and each SRAM device includes a write port and a read port to enable data to be written to and read from each SRAM device simultaneously.

8. In a multiport switch that controls communication of data frames between stations and includes a plurality of queues corresponding to ports on the multiport switch, a method of processing data frames, comprising:

receiving data frames at a plurality of receive devices;

transmitting the data frames to an external memory interface;

writing frame header information from the data frames to a plurality of queues corresponding to the plurality of receive devices, wherein the plurality of queues are formed on a memory device that includes a write port and a read port;

allocating time slots to the plurality of queueing devices;

transmitting the frame header information from the queues, via the read port and in successive time slots, to an internal decision making engine; and

generating data forwarding information.

9. The method of claim 8, comprising:

allocating time slots based on a predetermined priority; and

transmitting frame header information during the allocated time slots.

10. The method of claim 9, comprising:

transmitting a request signal to a scheduler, the request signal indicating that a first queue has stored frame header information.

11. The method of claim 10, comprising:

assigning at least one time slot in a scheduling cycle to each of the plurality of queues; and

allocating the time slot assigned to a first queue when the request signal has been received.

12. The method of claim 8, wherein the frame header information comprises a source address and a destination address of the data frame.

13. The method of claim 9, wherein the frame header information comprises virtual local area network (VLAN) information.

14. A multiport switch configured for controlling communication of data frames between stations, comprising:

a plurality of receive devices corresponding to ports on the multiport switch, each of the receive devices configured to receive data frames and transmit the data frames on an internal bus to an external memory interface;

a plurality of queues corresponding to ports on the multiport switch, the plurality of queues formed on a memory device that includes a write port and a read port, wherein each of the plurality of queues is assigned at least one time slot in a scheduling cycle and is configured to store frame header information via the write port;

a scheduler configured to allocate time slots to the plurality of queues based on data traffic at the corresponding receive ports; and

a decision making engine configured to receive the frame header information in successive time slots via the read port and to generate data forwarding information.

15. The multiport switch of claim 14, comprising:

a memory controller configured to transfer frame header information from the plurality of queues to the decision making engine via the read port,

wherein the scheduler is configured to allocate the time slots based on a predetermined priority and the read controller is configured to transmit frame header information to the decision making engine during the allocated time slots.

16. The multiport switch of claim 15, wherein:

the memory controller is configured to transmit a request signal to the scheduler, the request signal indicating that a first queue has stored frame header information,

the scheduler is configured to allocate a time slot assigned to the first queue when the request signal has been received, and

the memory controller is configured to transmit the frame header information from the first queue to the decision making engine during the allocated time slot.

17. The multiport switch of claim 14, wherein

the frame header information comprises a source address, and a destination address of the data frame.